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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/760,380 | 01/21/2004 | Fumitoshi Ito | 501.40147CX2 | 9832 |

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| EXAMINER | |
|---|---|
| SCHILLINGER, LAURA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/760,380 | ITO, FUMITOSHI | |
| | Examiner | Art Unit | |
| | Laura M. Schillinger | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-19,23 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al (148).

20. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate (Fig.10 (layers 1 and 2));

a plurality of static random access memory (SRAM) cells, disposed on the substrate each having a pair of n-channel drive metal insulator semiconductor field effect transistors (MISFETS), a pair of p-channel load MISFETS and a pair of n-channel selection MISFETS (Abs., lines: 1-5 and $Q_{1, 2, s1, s2}$) wherein the n-channel drive MISFETS and n-channel selection MISFETS contain a lightly doped drain (LDD) structure (Col.5, lines: 40-50), respectively, wherein the p-channel load MISFETs have a source, a drain and a gate electrode respectively (Fig.9 (7D); wherein the p-channel load MISFETS contain a single drain structure, respectively (Fig.6 (10) and Col.9, lines: 25-30), and

wherein the drain and source of each p-channel load MISFET are formed inside the semiconductor substrate ((Fig. 9 (2)).

21. (Previously Presented) A semiconductor integrated circuit device according to claim 20, wherein each one of the n-channel drive MISFETS is coupled with one of the p- channel MISFETS to form an inverter circuit (Col.4, lines: 1-10).

22. (New) A semiconductor integrated circuit device according to claim 20, wherein each of drain regions of the n-channel drive MISFETS and n-channel selection MISFETS is comprised of a first region and a second region, the first region has an impurity concentration of dopant greater than that of the second region, and each of the second regions of the n-channel drive MISFETS and n-channel selection MISFETS is disposed nearer to each of gate electrodes of the n-channel drive MISFETS and n-channels selection MISFETS than is the first region (Col.5, lines: 40-65).

***Response to Arguments***

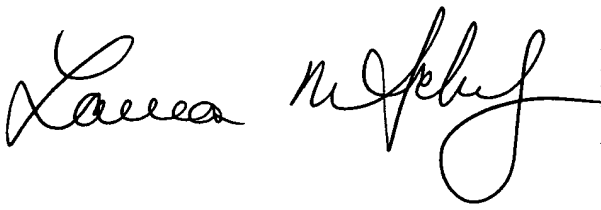
Applicant's arguments filed 6/14/06 have been fully considered but they are not persuasive. Applicant argues that Ikeda fails to teach the source and drain structures of the p-channel load MISFETs are formed inside a substrate. However as shown in Fig.9, both source and drains are formed within a well formed within the substrate (Col.4, lines: 50-55), therefore, Applicant's claim language is anticipated by Ikeda.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Laura M Schillinger
Primary Examiner
Art Unit 2813

8/3/06